



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,982	12/28/2001	Gurvant Patel	TI-33382	8689

7590

08/12/2003

Dennis Moore  
Texas Instruments Incorporated  
P.O. Box 655474, M/S 3999  
Dallas, TX 75265

EXAMINER

NGUYEN, VINCENT Q

ART UNIT

PAPER NUMBER

2858

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/032,982

Applicant(s)

PATEL, GUNVANT

Examiner

Vincent Q Nguyen

Art Unit

2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-15 is/are allowed.
- 6) ☒ Claim(s) 1-8, 16, 18, 19 and 21 is/are rejected.
- 7) ☒ Claim(s) 17 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 16, 18, 19, 21, are rejected under 35 U.S.C. 102(b) as being anticipated by Shoemaker (3,581,198).

Regarding claim 16, Shoemaker discloses a device comprising a first (12) and second node (13) and a pair of output terminals (11) (Even it is shown only one terminal, the output for the amplifier is a pair of output terminals); a first resistor (PBR23) coupled to said first node (12), and first resistor receiving a first input voltage (From 43); a second resistor (PBR24) coupled to said first node (12); a third resistor (PBR22) coupled to the said second node (13), said third resistor receiving a second input voltage; a fourth resistor (PBR21) coupled to said second node (13); and wherein said second resistor (PBR24) and said fourth resistor (PBR21) communicate a voltage at said first node (12) and said second node (13), respectively, that is indicative of the internal circuit continuity of said analog device (This is true not only for the prior art of Shoemaker, such as element 10, but also true for any other prior art having similar structure since at the node, if the current drawn into the device, there must be a voltage drop at the node, this indicates that the device is continuity).

Regarding claim 18, Shoemaker discloses said first input voltage comprises a negative voltage (Element 43 is inverting amplifier, thus the voltage at VCM must be a negative one).

Regarding claim 19, Shoemaker discloses said analog device is configured as a differential amplifier (10).

Regarding claim 21, Shoemaker discloses said analog device (10) has a pair of feedback circuits each providing feedback (26, 27), one said feedback circuit being coupled between each said output terminal and one said respective input terminal (See also figure 1b).

3. Claims 1, 4, 6, 8, are rejected under 35 U.S.C. 102(b) as being anticipated by Farmer (4,088,947).

Regarding claim 1, Farmer discloses a method comprising the steps of (Figure) providing a first voltage (-15V) via a first resistor (42) to said first node (46) using a first input of said test circuit; and measuring (Q1, Q2) a second voltage at the first node (46) via a second input (56) of said test circuit; wherein said measured second voltage is indicative of the internal circuit continuity of said analog device (36).

Regarding claim 4, Farmer discloses said second voltage is measured at said first node (46) without using a relay.

Regarding claim 6, Farmer discloses said first voltage is negative voltage (-15V).

Regarding claim 8, Farmer discloses said analog device is an operational amplifier (36).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2, 7, are rejected under 35 U.S.C. 103(a) as being unpatentable over Farmer (4088947).

Regarding claims 2, the only difference between Farmer and the invention claimed is that the claim recites said measured second voltage is a diode drop below ground when the analog device first node has continuity in place of the transistor Q1. It would have been obvious to one of ordinary skilled in the art at the time the invention was made to recognize that, although, the voltage of the transistor (Q1) and the diode as claimed, is different in polarity (i.e. the measured second voltage is a diode drop below ground while the  $V_{BE}$  of Q1 is  $>0.7V$ ), the transistor and the diode, as claimed, achieves the same function (i.e. conducting the current to detect the continuity of the amplifier under test). In order for the transistor Q1 to be conducted to measure the voltage at node 46, the base voltage must higher than  $V_{BE}$  (Usually  $0.7V$ ), and in order for a diode, as claimed, to be conducted, a voltage applying to the diode must less than  $V_D$  (Usually  $-6.8V$ ). Thus, the measured second voltage is a diode drop below ground when the analog device first node has continuity would achieve the same function like that of the transistor Q1.

Regarding claim 3, Farmer discloses the measured second voltage (46) is the

Art Unit: 2858

applied said first voltage (-15V) when said analog device first node (46) does not have continuity.

Regarding claim 7, Farmer discloses the step of simultaneously applying a third voltage (5V) to said second input node (Non-inverting) via a third resistor (34), and measuring (At terminal 12) a fourth voltage at said second node.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farmer (4088947) in view of Shoemaker et al. (3,581,198).

Regarding claim 5, Farmer does not disclose said second voltage is measured via a second resistor being in parallel with said first resistor. Shoemaker et al. discloses a system similar to that of Farmer and further discloses (Figure 1A) said second voltage (At node12) is measured via a second resistor (PBR24) being in parallel with said first resistor (PBR23). It would have been obvious to one of ordinary skilled in the art at the time the invention was made to recognize the desirability of modifying Farmer to incorporate the a second resistor being in parallel with said first resistor to measure the second voltage as taught by Shoemaker since the parallel connection would reduce the time for the measuring device to connect to the node to enhance the test process (See Shoemaker column's 1, lines 66-75).

***Allowable Subject Matter***

7. Claims 9-15 are allowed.

8. Claims 17, 20, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

9. Applicant's arguments filed July 25, 2003 have been fully considered but they are not persuasive.

In response to Applicant's remark that Shoemaker does not disclose the support for an analog device having a first and second input terminal comprising a first and second node and a pair of output terminals. It is not necessary for the prior art to disclose and support in every detail the element, which is common knowledge. A pair of output terminals is a typical feature for most of the difference amplifiers, for example, the one disclosed in figure 1 (Applicant admitted prior art).

In response to Applicant's remark that neither PBR24 nor PBR21 is used to communicate a voltage at said first and second node. The examiner does not see why PBR24 and PBR21 are not used to communicate at the first node (12) and second node (13)? Generally in a circuit, every element must participate or communicate in order to perform a desired function. The circuit disclosed in figure 1A of Shoemaker is not an exception. PBR24 communicates a voltage with node (12) and PBR21 communicates a voltage with node (13) (It is noted that, across a resistor, there always has a potential different when current flows).

In response to Applicant's remark that the examiner fails to identify the element in Farmer that corresponds to the claimed "first input of the test circuit". Applicant also states that element 56 in Farmer is output of the operation amplifier, not a second input of the test circuit. Regarding claim 1, the limitation recites the steps which read on Farmer as examiner interpreted as follow: Providing a first voltage (-15V) via a first resistor (42) to said first node (46) using a first input of said test circuit; and measuring (Q1, Q2) a second voltage at the first node (46) via a second input (56) of said test circuit; wherein said measured second voltage is indicative of the internal circuit continuity of said analog device (36). The examiner is not understood what is meant by "the examiner fails to identify the element in Farmer that corresponds to the claimed"? Why element 56 in Farmer is not a second input of the test circuit? The fact is that the test circuit, as applied in the rejection, is the figure disclosed in Farmer. Because the claim does not specifically limit the second input of the test circuit, output signal of amplifier 36, which biases the base of Q1, is interpreted as a second input of the test circuit.

In response to Applicant remark that no arrangement suggested by Farmer results in the second voltage being a diode drop below ground. As the examiner discussed in the rejection (e.g. claim 2), although, the voltage of the transistor (Q1) and the diode as claimed, is different in polarity (i.e. the measured second voltage is a diode drop below ground while the  $V_{BE}$  of Q1 is  $>0.7V$ ), the transistor and the diode, as claimed, achieves the same function (i.e. conducting the current to detect the continuity of the amplifier under test). In order for the transistor Q1 to be conducted to measure



the voltage at node 46, the base voltage must higher than  $V_{BE}$  (Usually 0.7V), and in order for a diode, as claimed, to be conducted, a voltage applying to the diode must less than  $V_D$  (Usually -6.8V). Thus, the measured second voltage is a diode drop below ground when the analog device first node has continuity would achieve the same function like that of the transistor Q1.

### ***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

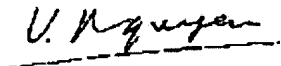
### ***Contact Information***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Q Nguyen whose telephone number is (703) 308-6186. The examiner can normally be reached on Mon-Fri 8:30-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vincent Q. Nguyen can be reached on (703) 308-6186. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-5841 for regular communications and (703) 308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vincent Q. Nguyen



August 8, 2003



N. Le  
Supervisory Patent Examiner  
Technology Center 2800